UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,242	08/30/2001	Wen Lin	00-LM-117	9379

7590   12/22/2004

Lisa K. Jorgenson, Esq.
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006

EXAMINER
CHOI, WOO H

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/943,242	LIN, WEN
	Examiner	Art Unit
	Woo H. Choi	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>28 October 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-27 and 31</u> is/are pending in the application.

4a) Of the above claim(s) <u>23-27</u> is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-22 and 31</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All   b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2.   Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention. Claim 31 depends from a cancelled claim. The scope of this claim is not clear.

Applicant is reminded that the listing of claims should list all claims including the

cancelled claims.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4.   Claims 1, 5 – 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanenbaum

(Operating Systems, Design and Implementation, Prentice-Hall, 1987).

5.   With respect to claims 1, 5, 6 and 11, Tanenbaum discloses a computing system (page

114, figure 3-3) comprising:

        a processor (CPU) having a data/control bus interface;

        a data/control bus (System bus) implementing one or more device communication

channels;

        a data memory (Memory) coupled to the processor;

        a mass storage device (Drive) having an interface for communicating mass storage

transactions; and

        a controller (Disk controller with DMA) having a memory interface coupled to the data

memory (interface to the system bus) and a mass storage interface (interface to the drive)

coupled to the mass storage device's interface and operable to conduct mass storage transactions

between the data memory and the mass storage device.

6.   With respect to claim 7 the system further comprising storage controller processes (page

92, disk task) and application behavior processes implemented using the processor (page 92,

other task, for example, terminal, memory, clock, file system, and user programs).

7.   With respect to claims 8 and 9 the storage controller processes map storage requests

generated by the application behavior processes expressed in logical geometry terms into storage

requests expressed in physical geometry terms (page 118, 3.2.3. Device Drivers, given a request

to read a block, block n for example, the device driver figures out where on the disk the

requested block actually is, see also pages 482 – 484).

8.   With respect to claim 10, the processor implements data structures storing physical

geometry information about the mass storage device (pages 482 – 484).

9.   With respect to claim 31, the storage related instructions include instructions

implementing read channel functionality (page 485, do_rdwt function).

10.   Claims 1 – 4 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunaker

(US Patent Application Pub. No. 2003/0036198).

11.   With respect to claim 1, Hunsaker discloses a computing system (figure 1) comprising:

        a processor having a data/control bus interface (processor 110);

        a data/control bus (host bus 120) implementing one or more device communication

channels;

        a data memory (system memory 140) coupled to the processor;

        a mass storage device (hard drive,176, floppy, 174, and CD ROM 172) having an

interface for communicating mass storage transactions; and

        a controller (memory controller hub 130, or alternatively, MHC 130 and ICH 150) having

a memory interface coupled to the data memory and a mass storage interface coupled to the

mass storage device's interface and operable to conduct mass storage transactions between the

data memory and the mass storage device.

12.   With respect to claim 2, the data memory is coupled to the processor by a memory bus

(system memory 140 is coupled to the processor via its own memory bus through the controller

130) operating independent of the data/control bus (the host bus 120 and the unlabeled memory

bus are independent buses). The Examiner notes that the only configuration where there are two

busses directly coupled to the processor is the one shown in figure 6. However this

configuration does not meet the controller requirements of claim 1.

13.   With respect to claim 3, the controller comprises a memory access controller coupled to

the processor, the data memory, and the mass storage device and operable to arbitrate accesses to

the data memory between the mass storage and the processor (the controller MHC 130 controls

access to the system memory and is the nexus that connects all of the claimed elements).

14.   With respect to claim 4, the controller comprises a direct memory access controller (page

2, paragraph 19) coupled to the data/control bus, wherein the mass storage interface comprises a

logical connection formed using one of the device communication channels.

15.   With respect to claim 21, the mass storage device comprises an optical storage device

(CD ROM 172).

16.   Claims 1, 12, 13 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaidi

et al. (US Patent No. 6,601,126, hereinafter "Zaidi").

17.   With respect to claim 1, Zaidi discloses a computing system (figure 28) comprising:

        a processor having a data/control bus interface(CPU);

        a data/control bus (CPU bus) implementing one or more device communication channels;

        a data memory coupled to the processor (DRAM);

        a mass storage device (DMA peripheral, see col. 27, lines 41 – 45) having an interface for

communicating mass storage transactions; and

        a controller (bridge and MAC) having a memory interface coupled to the data memory

and a mass storage interface coupled to the mass storage device's interface and operable to

conduct mass storage transactions between the data memory and the mass storage device.

18.   With respect to claim 12, (figure 1, and col. 4, lines 27 – 46, figure 28 is one of the

embodiments of this system on chip) the controller is integrated with the processor on a single

integrated circuit chip.

19.   With respect to claim 13, the mass storage device's interface comprises a peripheral

component interconnect (PCI) standard-compliant interface (figure 28).

20.   With respect to claim 20, the computing device comprises a network appliance (col. 27,

lines 40 – 45, in a networking application one of the DMA peripherals would be a network

controller) having a network controller coupled to the data/control bus.

21.   Claims 1, 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriarty

et al. (US Patent No. 6,128,669, hereinafter "Moriarty").

22.   With respect to claims 1 and 14, Moriarty discloses a computing system (figure 1)

comprising:

    a processor having a data/control bus interface(100);

    a data/control bus (102) implementing one or more device communication channels;

    a data memory coupled to the processor (104, or alternatively 112);

    a mass storage device (144) having an interface for communicating mass storage

transactions; and

    a controller (106, or alternatively 106 and 108) having a memory interface coupled to the

data memory and a mass storage interface coupled to the mass storage device's interface and

operable to conduct mass storage transactions between the data memory and the mass storage

device.

23.   With respect to claim 20, computing device comprises a network appliance having a

network controller coupled to the data/control bus (network controller 128 is coupled to 102

through 106).

24.   Claims 1, 13 – 16, and 20 – 22 are rejected under 35 U.S.C. 102(e) as being anticipated

by Yiu *et al.* (US Patent Application Pub. No. 2003/0181205, hereinafter "Yiu").

Yiu discloses a computing system (figure 3) comprising:

a processor having a data/control bus interface(31);

a data/control bus (41) implementing one or more device communication channels;

a data memory coupled to the processor (33);

a mass storage device (34) having an interface for communicating mass storage

transactions; and

a controller (page 3, paragraph 34) having a memory interface coupled to the data

memory and a mass storage interface coupled to the mass storage device's interface and operable

to conduct mass storage transactions between the data memory and the mass storage device.

Yiu discloses various interfaces claimed in claims 13 – 16 (page 3, paragraph 34), and

mass storage types claimed in claims 21 – 22 (page 3, paragraph 35). A network controller of

claim 20 is disclose as well (figure 3,37 – 38, page 3, paragraph 36)

25.   Claims 1 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellison *et al.*

(US Patent Application Pub. No. 2002/0144121, hereinafter "Ellison").

Ellison discloses a computing system (figure 1C) comprising:

a processor having a data/control bus interface (processor 110);

a data/control bus (host bus 120) implementing one or more device communication

channels;

a data memory (system memory 140) coupled to the processor;

a mass storage device (hard drive,176, floppy, 174, and CD ROM 172) having an

interface for communicating mass storage transactions; and

a controller (memory controller hub 130, or alternatively, MHC 130 and ICH 150) having

a memory interface coupled to the data memory and a mass storage interface coupled to the

mass storage device's interface and operable to conduct mass storage transactions between the

data memory and the mass storage device.

The computing device comprises a set-top box including processes for implementing

audio/video behaviors in the processor (page 1, paragraph 13).

26.   Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Houston *et*

al. (US Patent No. 6,493,656, hereinafter "Houston").

Houston discloses a computing system (figure 1) comprising:

a processor (100) having a data/control bus interface;

a data/control bus (104) implementing one or more device communication channels;

a data memory (106) coupled to the processor;

a mass storage device (118, 122) having an interface for communicating mass storage

transactions; and

a controller (102, or 102 and 114, or 102 and 121) having a memory interface coupled to

the data memory and a mass storage interface coupled to the mass storage device's interface and

operable to conduct mass storage transactions between the data memory and the mass storage

device.

wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in

response to commands (col. 1, lines 37 – 52);

a servo controller coupled to receive requests transferred from the data memory by the

controller and generate the commands to the actuator mechanism (figure 2).

27.   With respect to claim 18, the mass storage device's interface is implemented by the servo

controller and implements a physical interface to the data/control bus and a physical interface to

the head and actuator mechanism (col. 5, lines 27 – 37).

Response to Amendment

28.   Claims 28 – 30 have been cancelled.

29.   Claims 19 – 22 have been amended to overcome objections. Corresponding objections

are withdrawn.

Response to Arguments

30.   Applicant's argument filed October 28, 2004, with respect to the rejection, under 35

U.S.C 112, first paragraph, of claim 18 has been fully considered and is persuasive.

Corresponding rejection is withdrawn.

31.   Applicant's arguments filed October 28, 2004, with respect to the prior art rejections have

been fully considered but they are not persuasive.

32.   Tanenbaum teaches every claimed limitation as discussed above. As to claim 1,

Applicant's argument regarding the location of a DMA controller in Tanenbaum's teachings is

irrelevant as this is not a claimed feature. In addition, Tanenbaum specifically discloses, on page

114, that "Many controllers, especially those for block devices, support **direct memory access**

or **DMA**." The figure on the same page specifically shows DMA registers located in the disk

controller. As to Applicant's argument regarding Tanenbaum's disk controller having only an

interface to the system bus, the claim merely requires "a controller having a memory interface

coupled to the data memory." The figure clearly shows that the disk controller is coupled to the

data memory through the system bus, i.e. "a memory interface". The disk controller's interface

to the system bus is the interface through which the disk controller is coupled to the data

memory. The claims does not require that this memory interface be exclusively used to couple

to the data memory. It merely requires that it couples to the data memory.   Applicant's

allegations regarding other dependent claims, Applicant merely alleges that Tanenbaum does not

teach certain limitations without presenting any evidence or argument as to why the

corresponding teachings specifically pointed out in the rejections do not correspond to the

claimed limitations. Mere allegations do not overcome properly made rejections.

33.   With respect to Applicant's argument regarding Hunsaker reference, again Applicant

relies on features that are not claimed. Firstly, figure 1 of Hunsaker's disclosure clearly shows a

memory controller 130 that is coupled to the system memory 140, it also shows that it is coupled

to the mass storage device 170 through an interface that is separate from the one that is coupled

to the system memory via 150. The claim does not require that the controller be **directly**

coupled. Secondly, there's no requirement that the controller be implemented in a single device.

There is nothing improper about making an alternate rejection based on a combination of devices

to reject broadly stated claims when such a combination discloses all of the limitations of the

claims and the claims do not preclude such a combination. In addition, even if such a

combination is precluded by the claims, integrating functions of multiple devices into a single

device is generally considered obvious and not patentable unless there is sufficient evidence of

non-obviousness.

34.   As to Zaidi's disclosures, the bridge is clearly identified as the controller. Applicant has

not specifically and convincingly argued why this bridge does not read on the claimed controller.

Again there is no requirement for **direct** coupling of data memory to the processor. Regarding

the bridge's capability of conducting mass storage transactions, the transactions between the

memory and a DMA peripheral must go through the bridge. The claimed limitation is "operable

to conduct." One of the dictionary definitions of operable is *fit, possible, or desirable to use.*

One of the definitions of conduct is *to convey in a channel.* One of the other definitions is to

guide. The bridge is fit for conveying the mass storage transactions.

35.   As to Applicant's argument with respect to Moriarty and Ellison references, these

arguments have been discussed above.

36.   Applicant's non-enable argument regarding Yiu reference is not persuasive. The

statement in the reference "... FIG. 3 is not intended to represent any one specific physical

arrangement", that Applicant relies on to "prove" that Yiu's disclosure is non-enabling, does not

prove that Yiu's disclosure is non-enabling. The statement seems to have been made to not tie

their invention to a specific physical embodiment. Figure 3 seems to represent a typical

environment for Yiu's invention with other possible variations. In the same paragraph, the

disclosure states "Variations of the described structure may be appropriate ..." Applicant's

inability to obtain today a mass storage device such as one shown in figure 3, does not prove that

Yui's invention was non-enabled at the time of their invention.

37.   As to Applicant's arguments regarding Houton's disclosure, these arguments have been

discussed above in reference to Zaidi's disclosure.

Conclusion

38.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The

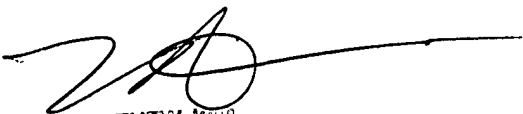examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc

December 14, 2004

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100